REMARKS

At the outset, the undersigned attorney wishes to thank the Examiner for his time and assistance in the prosecution of the instant application.

A replacement drawing including FIGS. 2 and 3 is submitted herewith. FIG. 3 has been corrected to show the designated width of line 205 and 215, and the designated width of separation 220. This correction to FIG. 3 corresponds to the original informal drawings of this application. No new matter has been added.

Claims 1, 8, 14 and 20 are currently amended. Claims 21 and 22 have been cancelled. Claims 23 and 24 have been added. Claims 1, 3-8, 10-14, 16-20 and 23-24 are pending. Claims 1, 8, 14 and 20 are the independent claims.

Claims 4, 5, 11, 12, 17 and 18 are objected to for failing to further limit the subject matter of their independent parent claims. These contentions have been obviated by the current amendments to claims 1, 8, 14 and 20, the independent parent claims.

Claim 14 was objected to for reasons stated on page 2 of the Office action. This contention has been obviated by the current amendments to Claim 14.

Claims 1, 3, 7, 8, 10, 14, 16, and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boaz et al. [6,061,263 A; hereinafter Boaz] in view of Kumakura et al. [US Patent No. 6,114,751 A; hereinafter Kumakura], Applicant Admitted Prior Art [hereinafter AAPA] and Perino et al. [US Patent No. 6,160,716 A; hereinafter Perino]. Claims 6, 13, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boaz in view of Kumakura, AAPA and Perino; as applied to claims 1,3,7,8,10,14,16 and 20-22 above, and further in view of Holman et al. [US Patent No. 6,005,776 A; hereinafter Holman]. Claims 1, 3-8, 10-14, and 16-22, as previously presented, stand rejected under 35 USC 103(a) under various combinations of cited prior art and alleged AAPA. These contentions have been obviated by the claim amendments that are made herein.

The present application describes routing a signal line through a single layer of a multi-layer circuit board between a memory control unit and a memory unit where the memory unit is connected to a signal line by pins (see, e.g., page 2, line 21 through page 3, line 4). The applicant found that a gap formed between neck down portions of each signal line provides an isolation between the signal lines yet reduces the area required to route the signal lines on a circuit board. Placing the gap, and not a ground trace, between the neck down portions may reduce congestion at the memory unit. This allows the signal

lines into and out of the memory unit to be routed through a single layer of the circuit board on which both the memory control unit (MCU) and the memory unit reside (page 4, lines 13-17). Routing the signal lines in this manner may reduce the number of layers required to route signals between the MCU and the memory unit by a factor of two. As a result, the circuit board on which the MCU and memory unit reside can be less expensive to produce than conventional memory boards. One description of a computer system is given on page 2, line 19 through page 3, line 4. Another description of a computer system is given on page 4, lines 15-17.

Consider exemplary independent claim 1, as currently amended, which recites in relevant part: "A computer system comprising: a circuit board comprising: … a first signal line, formed on a first layer of the circuit board and connected between a first pin on the memory unit and the memory control unit; and a second signal line also formed on the first layer of the circuit board and connected to the first pin on the memory unit, a first portion of the second signal line at an acute angle relative to a first portion of the first signal line,

a second portion of the second signal line substantially parallel to a second portion of the first signal line,

wherein said first layer defines a non-grounded gap between said first and second lines."

In contrast, Boaz teaches two separate boards, i.e., motherboard 10 and RIMM board 17 that are connected through an edge connector 19, i.e., a motherboard 17 that includes a plurality of edge connectors 19, and a plurality of memory module boards 14 that are inserted (and connected) to each of the edge connectors 19 (col. 2, lines 36-57). Moreover, Boaz describes the memory controller 15 as being connected to motherboard 10 and memory chip 21 being connected to a memory module board 17. Therefore, Boaz cannot properly be characterized as describing "A computer system comprising: a circuit board comprising: at least two layers formed in parallel to a surface of said circuit board, a first signal line, formed on a first layer of the circuit board and connected between a first pin on the memory unit and the memory control unit; and a second signal line also formed on the first layer of the circuit board and connected to the first pin on the memory unit", as recited by Applicant's exemplary claim 1.

Applicant also wishes to clarify the features of the prior art system shown on Fig. 2 of the application. The Applicant describes the prior art system of Fig. 2 that includes a "signal line 150 [that] *narrows*, or "necks down", to a width of approximately 5 mils. The signal line 160 exiting the pin 155 also has a width of approximately 5 mils before *expanding* to a width of approximately 18 mils." (page 2, lines 7-10 of the

application.) That is, Fig. 2 shows the tapering of signal lines 150 and 160, and is further supported by the application which describes the signal lines 150 and 160 as *narrowing* and/or *expanding* to the connection point 155. Furthermore, Fig. 2 shows a ground trace 165 that is required to separate the neck down portion of the signal lines 150, 160. The ground trace typically must be formed on different layers of the circuit board than the signal lines, therefore increasing the number of layers required on the circuit board. Nowhere in the prior art system of Fig. 2 is it shown or suggested that a circuit board comprises "a first portion of the second signal line at an acute angle relative to a first portion of the first signal line, a second portion of the second signal line substantially parallel to a second portion of the first signal line, wherein said first layer defines a non-grounded gap between said first and second lines", as recited by Applicant's claim 1.

Claims 8, 14 and 20 are the other independent claims. Claims 8, 14 and 20 are currently amended.

Consider exemplary independent claim 8, as currently amended, which recites in relevant part: "A method for use in routing signals... comprising: delivering a first signal over a first signal line on a first layer ... connected between the memory control unit and a first pin on the memory unit; delivering a second signal over a second signal line formed on

the first layer ... connected to the first pin of the memory unit, a first portion of the second signal line formed at an acute angle relative to a first portion of the first signal line, a second portion of the second signal line formed substantially parallel to a second portion of the first signal line, separating said first and second signal lines without a ground connection therebetween." None of the art of record discloses or suggests the combination of features recited in independent claim 8.

Consider exemplary independent claim 14, as currently amended, which recites in relevant part: "A method for use in manufacturing a computer system ... comprising: forming ... first and second signal lines on a first layer of the board; connecting a memory unit to the board such that a first pin on the memory unit connects to the first and second signal lines;... forming a first portion of the second signal line to be at an acute angle relative to a first portion of the first signal line; and forming a second portion of the second signal line to be substantially parallel to a second portion of the first signal line." None of the art of record discloses or suggests the combination of features recited in independent claim 14.

Consider exemplary independent claim 20, as currently amended, which recites in relevant part: "A circuit board comprising at least two layers ... a first signal line formed on a

first layer of the circuit board and connected to the memory control unit and to a first pin on the memory unit; and a second signal line formed on the first layer of the circuit board and also connected to the first connection on the memory unit, a first portion of the second signal line at an acute angle relative to a first portion of the first signal line, a second portion of the second signal line substantially parallel to a second portion of the first signal line, wherein the widths of the lines and the distance separating the lines are each substantially equal, and wherein said first layer defines a non-grounded gap between said first and second lines." None of the art of record discloses or suggests the combination of features recited in independent claim 20.

In view of the foregoing distinctions, Applicant respectfully submits that independent claims 1, 8, 14 and 20 are patentably distinguishable over the cited art. Applicant respectfully submits that claims 1, 8, 14 and 20 are in condition for allowance, and Applicant respectfully requests allowance of claims 1, 8, 14 and 20.

Claims 3-7, 10-13, 16-19 and 23-24 depend either directly or indirectly from one of the independent claims. Each dependent claim further defines the independent claim from which it depends. In view of the foregoing remarks regarding claims 1, 8, 14 and 20, Applicant respectfully submit that claims 3-7,

10-13, 16-19 and 23-24 are likewise in condition for allowance. Applicant respectfully requests allowance of claims 3-7, 10-13, 16-19 and 23-24.

Accordingly, all of the pending claims are now in condition for allowance. A formal notice to that effect is respectfully solicited.

If, in the Examiner's opinion, a telephonic interview would expedite the favorable prosecution of the present application, the undersigned attorney would welcome the opportunity to discuss any outstanding issues and to work with the Examiner toward placing the application in condition for allowance.

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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